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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/560,223	12/12/2005	Haruhiko Ikeda	36856.1394	2555

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EXAMINER	
SCARLETT, SHAKA S	

ART UNIT	PAPER NUMBER
2823	

NOTIFICATION DATE	DELIVERY MODE
03/19/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/560,223	IKEDA, HARUHIKO	
	Examiner	Art Unit	
	SHAKA SCARLETT	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 October 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *8-13* is/are pending in the application.

4a) Of the above claim(s) *13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *8-10* is/are rejected.

7)☒ Claim(s) *11 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. (US 6,625,037 B2) in view of Suzuki (US 5,877,550).

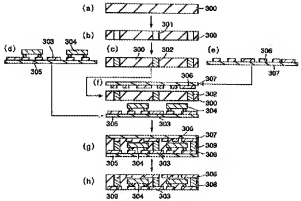


FIG. 3

Regarding Claim 8, Nakatani et al. discloses a process for producing a component-embedded substrate, comprising the steps of: connecting and fixing a first electronic component (304) to a first electrode pattern (303) on a first supporting layer (305) with a conductive bonding material (Column 10, line 30 – 33; Column 9, line 13 – 15); press-bonding a second supporting layer (307) including a second electrode pattern (306) onto the electronic component-fixed surface (304)) of the first supporting layer (305) with a first prepreg (300) there-between to perform transfer (Column 10, line

42 – 45, line 51 – 56); separating the first supporting layer (305) and the second supporting layer (307) from the first prepreg (300) such that the first and second electrode patterns (303, 306) are disposed on a front surface and a back surface of the first prepreg (300) (Column 10, line 64 - 65); curing the first prepreg before or after the step of separating the first supporting layer and the second supporting layer from the first prepreg (Column 10, line 51 – 56); connecting and fixing a second electronic component onto a back surface of the second electrode pattern (306) (Column 11, line 7 – 10). Nakatani et al. discloses a multi-layer device constructed of a plurality of layers including electronic components mounted on electrodes with a prepreg in-between (see Fig. 4), wherein the electrodes are used for mounting electronic components and prepreg material (401b) is formed in-between. However, Nakatani et al. does not explicitly disclose connecting and fixing a second electronic component onto a back surface of the second electrode pattern with a conductive bonding material after the step of curing the first prepreg; press-bonding a third supporting layer including a third electrode pattern onto a second electronic component-fixed surface with a second prepreg there-between to perform transfer; separating the third supporting layer from the second prepreg; and curing the second prepreg before or after the step of separating the third supporting layer from the second prepreg, wherein the prepregs and the electrode patterns are sequentially laminated. Rather, Nakatani et al. discloses forming built-in modules in clusters.

However, Suzuki discloses a process for producing a component-embedded substrate comprising forming an electronic component (3) on a substrate (1) having an

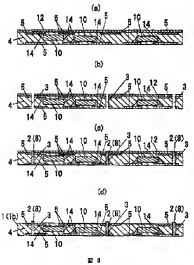
electrode pattern (2) formed thereon, forming an insulating layer 6 and a resin layer on the support substrate (1), forming a second electronic component on a second electrode pattern (Fig. 4), and repeating the process of embedding the second electronic component (3). Suzuki discloses a process of embedding an electronic component involving a sequential process of continually building up embedded electronic components to form a multi-layered structure.

Therefore it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify forming a built-in module using the process illustrated in Fig. 3 with a second electronic component on the electrode 306 (Column 11, line 7 – 10) of Nakatani et al. with a sequential process of Suzuki as it would provide the motivation to form a multilayered structure by repeating the lamination process (MPEP 2144.07). Modifying Nakatani et al. with Suzuki would produce a structure wherein after bonding the second electronic component to electrodes (306) (Column 11, line 7 – 10), the process disclosed in Fig. 3 may be repeated by press-bonding a third support (Fig. 3 (f), 307)) with electrodes to the second electronic component fixed to electrode (306), curing, then releasing the support 307 to form a multilayered structure. The claim would have been obvious because a person of ordinary skill has good reason to pursue the known options within his or her technical grasp. If this leads to the anticipated success, it is likely the product not of innovation, but of ordinary skill and common sense (KSR International Co. v. Teleflex Inc., 82 USPQ2d 1385 (U.S. 2007)). The process of repeating a single process as disclosed in Suzuki for forming a multilayered component-embedded device is evident this process is well-known and

can be applied by one skilled in the art to other known methods and devices such as that disclosed in Nakatani et al.

3. Claims 9 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakatani et al. (US 6,625,037 B2) in view of Suzuki (US 5,877,550) and further in view of Baba et al. (US 2005/0118750 A1).

Regarding Claim 9, Nakatani et al. and Suzuki in combination fail to disclose the process for producing the component- embedded substrate according to claim 8, further comprising the steps of: forming a through hole in the first prepreg which extends in a thickness direction of the first prepreg after curing the prepreg; and forming a conducting path inside the through hole, the conducting path electrically connecting the first and second electrode patterns provided on the front surface and the back surface of the first prepreg.



However, Baba et al. teaches a method of producing a component-embedded substrate wherein a through hole (3) is formed in a prepreg (4) which extends in a

thickness direction of the prepreg after curing (Paragraph 0113, line 1 – 8; paragraph 0122, line 1 – 3), and forming a conducting path (8) inside the through hole (3), the conducing path electrically connects a first and second electrode pattern (5) provided on the front surface and the back surface of the prepreg (Paragraph 0123, line 1 – 9).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the invention of Nakatani et al. and Suzuki with forming conductive through-holes through the prepreg to connect the first and second electrodes as taught by Baba et al. as it would provide the motivation to form a conductive through-hole to connect electrodes and other components for electrical communication inside the prepreg and externally after the curing process so as to avoid deformation that would occur if the vias where formed before the curing process since the prepreg material is not hardened.

Regarding Claim 10, Nakatani et al. and Suzuki in combination fail to disclose the process for producing the component- embedded substrate according to claim 8, further comprising the steps of: forming a through hole in the first prepreg connecting the electrode pattern provided on the front surface or the back surface of the first prepreg with an external electrode of the first electronic component after curing the first prepreg; and forming the conducting path inside the through hole, the conducting path electrically connecting the electrode pattern with the external electrode of the first or second electronic component.

However, Baba et al. teaches a method of producing a component-embedded substrate wherein a through hole (3) is formed in a prepreg (4) which connecting the

electrode pattern (5) provided on the front surface or back surface of the first prepreg with an external electrode of an electronic component (10) after curing (Paragraph 0113, line 1 – 8; paragraph 0122, line 1 – 3), and forming a conducting path (8) inside the through hole (3), the conducing path electrically connects the electrode pattern (5) with the external electrode (14) of the electronic components (Paragraph 0123, line 1 – 9; paragraph 0084, line 1 – 7).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the invention of Nakatani et al. and Suzuki with forming conductive through-holes through the prepreg to connect the electronic devices with the electrode patterns as taught by Baba et al. as it would provide the motivation to form a conductive through-hole to form electrical connections to the electronic components and electrodes for external electrical communication after the curing process so as to avoid deformation that would occur if the vias where formed before the curing process since the prepreg material is not hardened.

Allowable Subject Matter

4. Claims 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

5. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 11, the limitations of "performing temporary curing before separating the first and second supporting layers from the first prepreg; and performing complete curing after separating the first and second supporting layers from the first prepreg" cannot be found alone or in combination in the prior art.

Regarding Claim 12, the limitations of "performing temporary curing before separating the third supporting layer from the second prepreg; and performing complete curing after separating the third supporting layer from the second prepreg" cannot be found alone or in combination in the prior art.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SHAKA SCARLETT whose telephone number is (571)270-3089. The examiner can normally be reached on Monday-Friday 7:30 AM - 5:00 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

March 13, 2008
/Shaka Scarlett/
Examiner, Art Unit 2823

/Julio J. Maldonado/
Examiner, Art Unit 2823